

UNCLASSIFIED

STRUCTURES (U) CINCINNATI UNIV ON SOLID STATE
ELECTRONICS LAB J T BOYD 15 MAY 84 AFOSR-TR-84-0777
AFOSR-81-0130 F/G 17/8

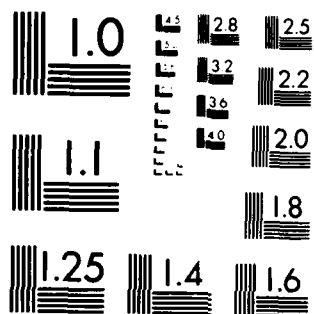
NL

END

DATE
EX MED

100

08.



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

AFOSR-TR-

②

Interim Report

AD-A146 278

INTEGRATION OF DETECTORS WITH
OPTICAL WAVEGUIDE STRUCTURES

J. T. Boyd

Solid State Electronics Laboratory
Department of Electrical and Computer Engineering
University of Cincinnati
Cincinnati, Ohio 45221

J. T. Boyd, Principal Investigator

Prepared for the:

Air Force Office of Scientific Research

Grant AFOSR-81-0130

May 15, 1984

RECEIVED
MAY 15 1984
AFOSR

Approved
for release

84 09 17 014

OTIC FILE COPY

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

AD-A146278

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified			1b. RESTRICTIVE MARKINGS		
2a. SECURITY CLASSIFICATION AUTHORITY			3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited.		
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE None			5. MONITORING ORGANIZATION REPORT NUMBER(S) AFOSR-TR.		
4. PERFORMING ORGANIZATION REPORT NUMBER(S)			7a. NAME OF MONITORING ORGANIZATION Air Force Office of Scientific Research		
6a. NAME OF PERFORMING ORGANIZATION University of Cincinnati		6b. OFFICE SYMBOL (If applicable)	7b. ADDRESS (City, State and ZIP Code) Bolling Air Force Base, D.C. 20332		
6c. ADDRESS (City, State and ZIP Code) Department of Electrical & Computer Engrg. Mail Location #30 Cincinnati, Ohio 45221			8a. NAME OF FUNDING/SPONSORING ORGANIZATION Air Force Office of Scientific Research		
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Air Force Office of Scientific Research		8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER AFOSR-81-0130		
8c. ADDRESS (City, State and ZIP Code) Bolling Air Force Base, D.C. 20332			10. SOURCE OF FUNDING NOS.		
			PROGRAM ELEMENT NO. 61102F	PROJECT NO. 2305	TASK NO. B1
11. TITLE (Include Security Classification) Integration of Detectors and Optical Waveguide Structures			12. PERSONAL AUTHOR(S) J. T. Boyd		
13a. TYPE OF REPORT Interim		13b. TIME COVERED FROM 3/15/83 TO 3/14/84	14. DATE OF REPORT (Yr., Mo., Day) 5/15/84		15. PAGE COUNT
16. SUPPLEMENTARY NOTATION					
17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)		
FIELD	GROUP	SUB. GR.	Integrated optics, optical waveguide, laser recrystallization.		
19. ABSTRACT (Continue on reverse if necessary and identify by block number)					
<p>Progress in several areas regarding the integration of photodetectors with optical waveguide structures is presented. In the area of formation of photodetector arrays on layers of laser-recrystallized polycrystalline silicon, progress has occurred in using antireflection stripes to control the location of grain boundaries. Large areas free of grain boundaries are then available for photodetector fabrication. A 6mm x 5mm test chip containing photodetector arrays, switching MOS transistors, and a number of other test devices has been designed and masks fabricated. This test chip has been fabricated with operation just demonstrated. Detailed testing of this chip is now underway. A second CMOS test chip containing over 1000 transistors which will allow us to evaluate use of CMOS signal processing circuitry with photodetector arrays on laser recrystallized silicon has been designed with mask fabrication beginning.</p> <p>In the area of SiO₂ waveguides, various variations in the thermal oxidation process are being evaluated for the purpose of creating very low loss waveguides. Loss values on</p>					
20. DISTRIBUTION/AVAILABILITY OF ABSTRACT UNCLASSIFIED/UNLIMITED <input checked="" type="checkbox"/> SAME AS RPT. <input type="checkbox"/> DTIC USERS <input type="checkbox"/>			21. ABSTRACT SECURITY CLASSIFICATION Unclassified		
22a. NAME OF RESPONSIBLE INDIVIDUAL Lt. Col Carter			22b. TELEPHONE NUMBER (Include Area Code) 555-427-4931	22c. OFFICE SYMBOL AFOSR/NE	

SECURITY CLASSIFICATION OF THIS PAGE

Accession For
NTIS
DTIC TAB
Unannounced
Justified
By
Distribution
Codes
A-1

SECURITY CLASSIFICATION OF THIS PAGE

Table of Contents

	Page
I. Introduction	1
II. SiO ₂ Optical Waveguides	3
A. Planar Waveguides	3
B. Channel Waveguides	7
III. Photodetectors formed in Laser Recrystallized Silicon	14
IV. Outlook - Progress with Regard to Objectives	21
V. Program Publications	22
VI. Acknowledgments	25
VII. References	26

I. Introduction

We are currently performing research under grant AFOSR 81-0130 involving integration of photodetector arrays with optical waveguide structures and applications to signal processing. This grant is continuing research initiated under grant AFOSR 76-3032; results from this earlier grant are described in the final report.¹ The present report summarizes progress achieved in Part III of this research program (March 15, 1983 - March 14, 1984). The main accomplishments resulting from research performed during this period include a number of accomplishments in the area of photodetectors formed in laser recrystallized silicon and continued progress on SiO_2 waveguides having very low scattering loss.²⁻⁴ In the area of SiO_2 waveguides progress has been achieved for both planar and channel waveguide configurations. Results in each of the above areas are discussed in the following sections.

The present research program has thus far investigated a number of integrated optical device configurations utilizing a silicon substrate. The motivation for investigating devices utilizing silicon is first, due to its potential use for such signal processing devices as the integrated optical spectrum analyzer,⁵⁻⁸ second, its usefulness for performing waveguide detection in such signal processing devices formed on LiNbO_3 , third, to provide structures useful for optical interconnections in very large scale integrated (VLSI) electronic circuits, fourth, to provide integration of external components in fiber optic interferometric devices,⁹ and fifth, to allow combination of integrated optical devices and integrated electronic circuits to

form higher data rate systems. The recent demonstration in our laboratory of waveguide loss in thin film waveguides as low as .01 dB/cm after laser annealing implies that it may be worthwhile considering formation of the interferometer in an optical waveguide rather than a fiber.⁹ Such a configuration would significantly reduce the size and allow total component integration on a silicon wafer substrate. This reduction in size and increase in component integration would be very desirable for application of guided wave interferometric sensors in military systems.

To support the overall goals of Air Force research, there has been significant interaction between personnel involved in the present and past AFOSR research program and those involved in military programs at the Air Force Avionics Laboratory, Rockwell International, McDonnell-Douglas, Battelle, Motorola, General Dynamics, Lockheed, Honeywell, and Oak Ridge National Laboratory. A number of papers have been co-authored by personnel from several of these institutions with personnel from the Solid State Electronics Laboratory at the University of Cincinnati.

The focal plane disector is a device structure which was originally conceived and first demonstrated by D. A. Ramey and J. T. Boyd of the University of Cincinnati working under AFOSR funding.^{10,11} This concept is now being contracted by the Air Force Wright Aeronautical Laboratories (Avionics Laboratory) to the Westinghouse Defense Electronics Center for development and use in optical signal processing systems.

II. SiO₂ Optical Waveguides

A. Planar Waveguides

A new type of planar optical waveguide consisting of a graded SiO₂ layer has been fabricated on silicon substrates. The expectation is that such planar waveguides would have many of the advantages of fibers, including low scattering loss. We have demonstrated such waveguides having low loss. These waveguides were formed by oxidizing silicon wafers under time-varying conditions. Our recent emphasis has been directed towards achieving stronger field confinement. By doing this we expect to be able to eliminate loss due to substrate coupling. Some progress in creating stronger field confinement has been obtained, but lower values of overall loss are still being sought.

During the past year, several sets of these SiO₂ planar waveguides were fabricated with the goal of improving the loss values obtained from previous SiO₂ planar waveguides. Taft¹² showed that the index of refraction of a layer of SiO₂ was dependent on the growth temperature and the water content of the ambient oxygen. His data has been used to develop processes which would give four layer planar waveguides. In the first experiment, the wafers were processed according to the schedule in Table Ia. Calculations from SUPREM¹³ and from Taft's data predicted that a waveguiding structure would result. Theoretical values for the loss based on the four layer slab waveguide model were calculated and compared to the loss obtained for the actual waveguide. As can be seen from the results, shown in Table IIa, the theoretical loss is lower than the value obtained from the loss measurement. Two possible reasons for this are the the isolation

Fabrication Process Sequences
for Various Samples

Table Ia

Sample #	Process
1,2	40 minutes wet oxygen, 1100 °C 600 minutes dry oxygen, 1100 °C 1860 minutes wet oxygen, 1000 °C 13440 minutes wet oxygen, 1100 °C
3,6	40 minutes wet oxygen, 1100 °C 600 minutes dry oxygen, 1100 °C 1860 minutes wet oxygen, 1000 °C 9128 minutes wet oxygen, 1100 °C
4,5	40 minutes wet oxygen, 1100 °C 600 minutes dry oxygen, 1100 °C 1860 minutes wet oxygen, 1000 °C 4800 minutes wet oxygen, 1100 °C

Table Ib

Sample #	Process
18	2820 minutes wet oxygen, 900 °C 600 minutes wet oxygen, 1100 °C
7	2820 minutes wet oxygen, 900 °C 1440 minutes wet oxygen, 1100 °C
8	2820 minutes wet oxygen, 900 °C 2880 minutes wet oxygen, 1100 °C
9	2820 minutes wet oxygen, 900 °C 4320 minutes wet oxygen, 1100 °C

10	2820 minutes wet oxygen, 900 ° C 5760 minutes wet oxygen, 1100 ° C
12	2820 minutes wet oxygen, 900 ° C 7200 minutes wet oxygen, 1100 ° C
13-18	2820 minutes wet oxygen, 900 ° C 8640 minutes wet oxygen, 1100 ° C

Table Ic

Sample #	Process
20	4320 minutes wet oxygen, 900 ° C
26	4320 minutes wet oxygen, 900 ° C 1440 minutes wet oxygen, 1100 ° C
23	4320 minutes wet oxygen, 900 ° C 4430 minutes wet oxygen, 1100 ° C
28	4320 minutes wet oxygen, 900 ° C 5870 minutes wet oxygen, 1100 ° C
25	4320 minutes wet oxygen, 900 ° C 7370 minutes wet oxygen, 1100 ° C
27	4320 minutes wet oxygen, 900 ° C 10130 minutes wet oxygen, 1100 ° C
30	4320 minutes wet oxygen, 900 ° C 13070 minutes wet oxygen, 1100 ° C
29	4320 minutes wet oxygen, 900 ° C 15950 minutes wet oxygen, 1100 ° C

24	4320 minutes wet oxygen, 900 ° C 18770 minutes wet oxygen, 1100 ° C
----	--

19,22	4320 minutes wet oxygen, 900 ° C 21700 minutes wet oxygen, 1100 ° C
-------	--

layer was not as thick as predicted by SUPREM so that there was stronger coupling to the substrate than we expected. Second, there is a possibility of a relaxation phenomenon occurring whereby the difference in the refractive index between the guiding layer and the isolation layer is not as large as that predicted by Taft's data. Third, the four layer model used for the calculations may not be adequate for the graded index structure.

It was decided try to fabricate new slab waveguides using the process shown in Table Ib. Loss measurements were made on these waveguides with the results shown in Table IIb. Again, the loss was considerably larger than that predicted by the four layer slab waveguide model. Oxide thickness was measured in order to ensure that the isolation layer thickness was sufficient to prevent strong coupling from the waveguide to the substrate. The oxide was found to be significantly thinner than that predicted by SUPREM and modifications were made to the oxidation system to improve the predictability of the thickness of the oxide layers. The experiment was then repeated using the process in Table Ic. Again, loss values were higher than predicted by the model as is shown in Table IIc. This time, oxide thickness measurements showed that the oxides were sufficiently thick to prevent coupling to the substrate. An experiment is now being designed to determine if the relaxation phenomenon mentioned above is causing these waveguides to exhibit losses much higher than is predicted by the model.

B. Channel Waveguides

We have explored several approaches to fabricating low-loss

Table II
Waveguide Loss for Various Samples
Listed in Table I

Table IIa. Waveguide Loss

Sample #	Measured Loss	Theoretical Loss
1	$-1.33 \pm .24$ dB/cm	$< .1$ dB/cm
2	$-0.92 \pm .11$ dB/cm	$< .1$ dB/cm
3	$-2.99 \pm .41$ dB/cm	$< .1$ dB/cm
6	$-1.35 \pm .19$ dB/cm	$< .1$ dB/cm
4,5	No guiding observed	

Table IIb. Waveguide Loss

Sample #	Measured Loss	Theoretical Loss
14	-5.3 dB/cm	$< .1$ dB/cm
15	-4.5 dB/cm	$< .1$ dB/cm

Table IIc. Waveguide Loss

Sample #	Measured Los	Theoretical Loss
29	$-1.66 \pm .12$ dB/cm	$< .1$ dB/cm
30	$-1.32 \pm .15$ dB/cm	$< .1$ dB/cm
24	$-0.58 \pm .33$ dB/cm	$< .1$ dB/cm
19	$-0.58 \pm .76$ dB/cm	$< .1$ dB/cm

channel waveguides using SiO_2 on silicon substrates. Very low-loss planar waveguides can be formed on silicon by its thermal oxidation. However to form channel waveguides it is necessary to alter the refractive index in well-defined regions by introducing impurities to raise or lower the refractive index or by etching ridges.

We investigated the formation of waveguides by deposition, and oxidation of polycrystalline silicon after appropriate doping. Layers of silicon were evaporated onto oxidized silicon substrates in an electron beam evaporator. Layer thicknesses ranged from 1-2 microns. These layers were then doped with phosphorous or boron as described below. Oxidation of the doped Si layer provides a silicon dioxide layer the refractive index of which depends on the type and amount of impurity incorporated in it. Phosphorous raises the refractive index of the oxide whereas Boron lowers it slightly.

In order to dope selected areas of the deposited silicon, it is necessary to provide a masking layer if a gaseous dopant source is used. Alternatively, doped glass layers may be appropriately patterned and employed as a dopant source. We used a combination of both approaches. In one case a borosilicate glass layer was chemically vapor deposited on the evaporated silicon layer. Openings in the form of channels about 25mm long and 250 microns wide were then cut in the borosilicate glass layer. The wafer was then exposed to an ambient containing phosphorous oxytrichloride (POCl_3) vapor. This enabled diffusion of Phosphorous into the channel regions and simultaneous diffusion of Boron into regions surrounding the channels. After diffusion, the glass layer was stripped in hydrofluoric acid.

Oxidation of the doped silicon layer was then carried out till it was completely converted to oxide. In a related approach phosphosilicate glass was chemically vapor deposited on the evaporated silicon layer and patterned into channels. The wafer was then heated in a nitrogen ambient for sixty minutes to drive phosphorous from the glass layer into the silicon layer. After this dopant drive in, the glass layer was etched off and the silicon layer oxidized to completion in oxygen bubbled through 97°C deionized water.

The results for both types of treatment were identical. The undoped or boron doped regions of the silicon layer resulted in smooth oxide layers. However, the phosphorous doped regions resulted in a very rough oxide surface. The difference in texture between the phosphorous doped channels and the background is dramatic. We believe that the rough surface is caused by enhanced growth of crystal grains in the evaporated silicon layer. It is well known that phosphorous enhances silicon grain growth whereas boron does not affect it significantly. Nonetheless, we did not encounter any reports in the literature that indicated the extent of surface roughening (visible to the unaided eye) that we observed.

Since the rough texture of the oxide obtained from Phosphorous-doped silicon makes it unsuitable for the fabrication of low loss waveguides, we decided to investigate the diffusion of germanium into silicon and subsequent oxidation. The presence of germanium also raises the refractive index of silicon dioxide. Furthermore, germanium and silicon are completely soluble in each other in all proportions, thus making it possible in theory to have a layer

composition ranging from 100% silicon to 100% germanium. In practice thermal oxidation of germanium is difficult since its oxide is not stable at the elevated temperatures required to achieve useful oxidation rates. We experimented by evaporating layers of silicon and germanium of different thicknesses such that a silicon/germanium mass ratio could be determined which allowed oxidation of the alloyed layer without deterioration. Typically, a thin layer of silicon was evaporated followed by a layer of germanium which was then patterned to form channels. Another layer of silicon was then evaporated on top of the patterned germanium layer. The wafer was then annealed in a nitrogen ambient. It was found that too large a fraction of germanium caused the layers to blister during annealing. Furthermore, the layers were damaged during oxidation at 1100 C. Eventually, we determined that a Si/Ge mass ratio of approximate 3.3 allowed the preparation of layers which could be oxidized safely. Samples were prepared in which this mass ratio existed in the channel regions and pure silicon in the surrounding areas. After oxidation, the waveguiding properties of the channels were tested. We found that guided modes could be supported in both the germanium doped channel regions as well as outside the channels. Furthermore, the modes were very lossy, probably due to coupling to the silicon substrate. These results indicated that the refractive index difference between the doped and undoped regions was quite small and further than much thicker oxide layers would have to be grown to prevent substantial coupling of the radiation to the substrate.

Next we attempted the fabrication of a thin film ring resonator using CVD phosphosilicate glass on top of thermal SiO_2 as the medium for forming the waveguide. The resonator is in the shape of a racetrack of perimeter approximately 5.14mm long and a linewidth of 4 microns. Four microns wide straight channels run on each side of the racetrack at a separation of 4 microns. The channel ends taper to a width of 70 microns to form input horns.

It was found that this pattern could not be transferred to the PSG using wet etching because of poor photoresist adhesion. The lithography process was modified to include a post-exposure bake and a post-develop exposure to improve photoresist adhesion. Then it was determined that wet etching was causing too much undercutting of the lines, so plasma etching was employed to transfer the pattern to the PSG. The first experiments involved etching ridges in a 3 microns thick PSG layer to form the resonator pattern. The time required to plasma etch through this thickness (20 minutes) was long enough that the photoresist film was destroyed in the process. So a wet-etch/plasma-etch combination was worked out to achieve the required etch depths. After etching the resonator pattern in the form of ridges of the PSG, the wafer was heat treated in a wet O_2 ambient to cause the glass to flow and thereby smooth out any rough edges and to decrease the gap between the coupling channel and the racetrack. The gap was then partially filled with borosilicate glass. In order to test the resonators light was coupled into the input channel and the wafer was heated. The racetrack of the resonator was expected to brighten and dim several times as it shifted through it's on-and off-

resonance conditions. Of the devices tested only one showed this behavior when the gap was further filled with index-making fluid. We have reasons to believe that there may be insufficient coupling between the input channel and the race track. This is because Phosphorous is depleted from the surface region of heavily doped phosphosilicate glass. This tendency is enhanced by high temperature and moisture. We therefore think that enough Phosphorous leaves the surface of the PSG ridges so as to cause a lowering of the refractive index substantial enough to lower the coupling coefficient.

Currently we are evaluating a slightly different approach to the fabrication of the resonator. This time we are using lower Phosphorous concentration PSG and etching grooves in it in the shape of the racetrack pattern. In this case any undercutting during etching would tend to narrow the dividing ridge between the input channel and the racetrack, thus allowing for enhanced coupling. The grooves will then be filled with more PSG and the wafer will be heat treated. This will allow phosphorous from the grooves to diffuse into the ridge separating the channel and racetrack thereby making the refractive index differences between these regions smaller. This should also enhance the coupling between the input channel and race track.

III. Photodetectors Formed in Laser Recrystallized Silicon

We are investigating the formation of photodetector arrays in laser recrystallized regions of silicon. The fabrication of photodetectors in such regions which have good performance will allow silicon detector arrays and associated circuitry to be integrated onto any optical waveguide substrate such as LiNbO_3 .

In working towards the above goal considerable preliminary work on laser recrystallization of polysilicon layers deposited on insulating substrates has taken place. Accomplishments in this area include:

1. Completed installation of facilities to allow unidirectional low speed scanning of the Argon laser.
2. Verified by experiment the reflection modulation of different thicknesses of silicon nitride layers on top of the polysilicon. See Table 3 for results.
3. Achieved limited success in duplicating the recrystallization of long single crystals by use of a pattern of anti-reflection silicon nitride stripes to control the location of grain boundaries. Figure 1 illustrates these results.
4. Achieved success in recrystallizing very long (.5 mm) but very narrow (20 microns) crystal grains in a .5 micron layer of polysilicon. It was also demonstrated that the argon laser beam used for heating the polysilicon would not effect the underlying waveguiding layer if recrystallization is done properly.
5. Automation of argon ion laser annealing apparatus allowing computer control of wafer positioning and movement in 3 axes,

Table III

SILICON NITRIDE THICKNESS -VS- MELTED LINE WIDTH

NITRIDE THICKNESS (ANGSTROMS)	MELTED LINE WIDTH (MICRONS)
620	30
560	47.5
500	50
440	58.5
380	65
320	67.5
260	67.5
200	64
140	54.5
80	34
20	-
0	-

WAFER	STRUCTURE:	TOP	SILICON NITRIDE	0-620	ANGSTROMS
			SILICON DIOXIDE	109	"
			POLYSILICON	3838	"
			SILICON NITRIDE	1045	"
			SILICON DIOXIDE	10114	"
			BULK SILICON		



Figure 1. Region free of grain boundaries in laser-recrystallized polysilicon.

control of laser power during during annealing, and control of a high power beam shutter.

6. Completed construction of a chamber allowing control of the gaseous or vacuum environment of samples being laser recrystallized or laser annealed.

Integrated optical photodiode arrays have been designed and fabricated on layers of laser recrystallized silicon. Currently, Si_3N_4 waveguides formed on SiO_2/Si substrates are serving as the insulating substrate for polysilicon deposition. An extensive photodiode array test chip has been designed to occupy a 6 mm x 5 mm chip. This chip contains several 40 element photodiode arrays, use of two different array element sizes, incorporation of switching MOSFETs for addressable readout, and a variety of test structures to evaluate both the processing and the laser recrystallization. Figure 2 illustrates the layout of the photodetector array test chip. Figure 3 illustrates the cross section of one element of the waveguide-detector structure. Operation of this test chip has just been demonstrated with detailed testing and evaluation now underway.

A separate test pattern that includes more than 1,000 transistors has been designed for testing the feasibility of fabricating CMOS circuits on laser recrystallized polysilicon layers. Development of such technology would allow integration of signal processing circuitry with photodetector arrays. Included in this test pattern are a 133 stage inverter array, a 17 stage ring oscillator, a 120 parallel transistor array, MOS capacitors, gate-controlled diodes, individual test transistors, and some other test structures. The process for

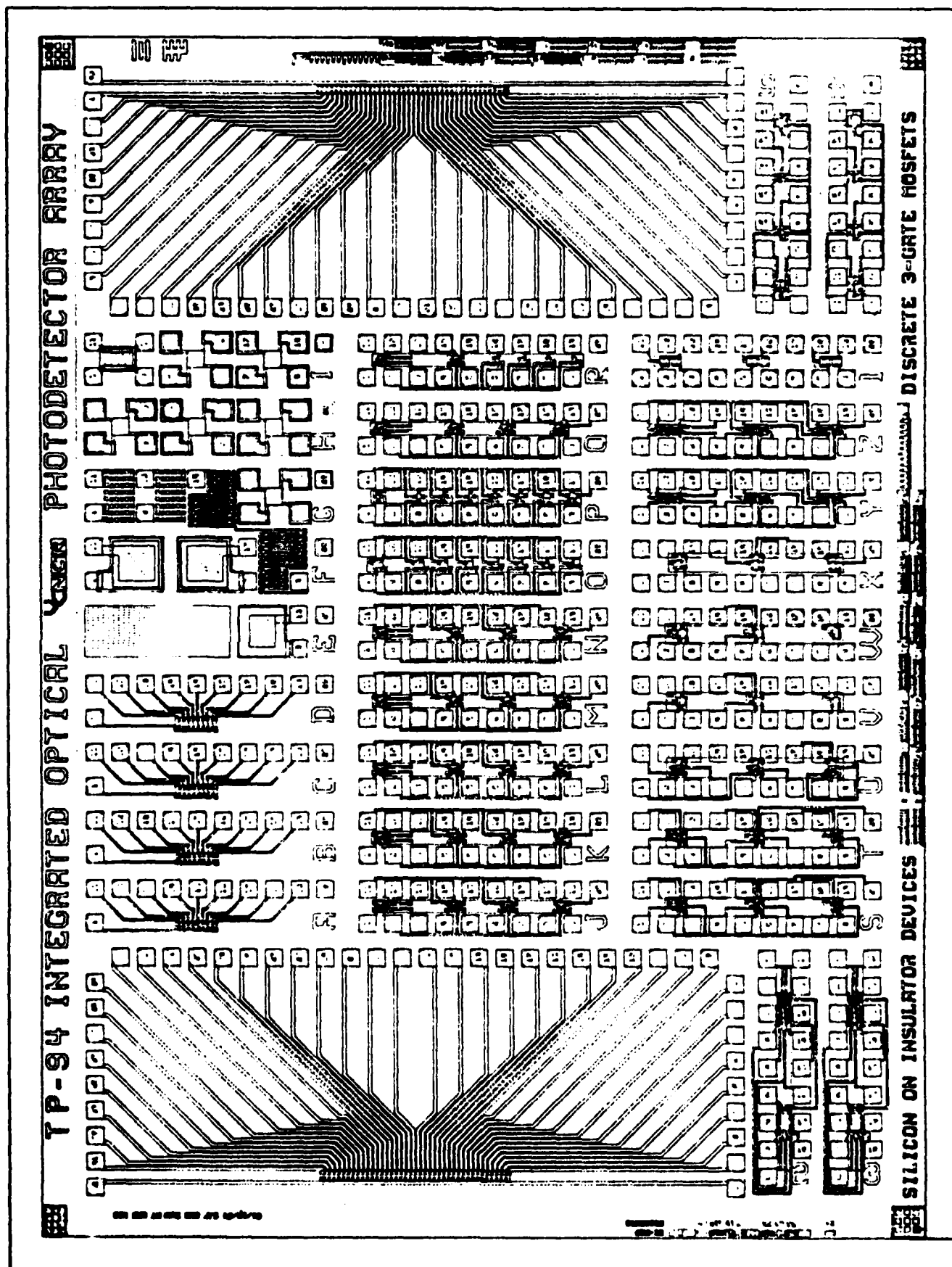


Figure 2. Photodetector array test chip layout.

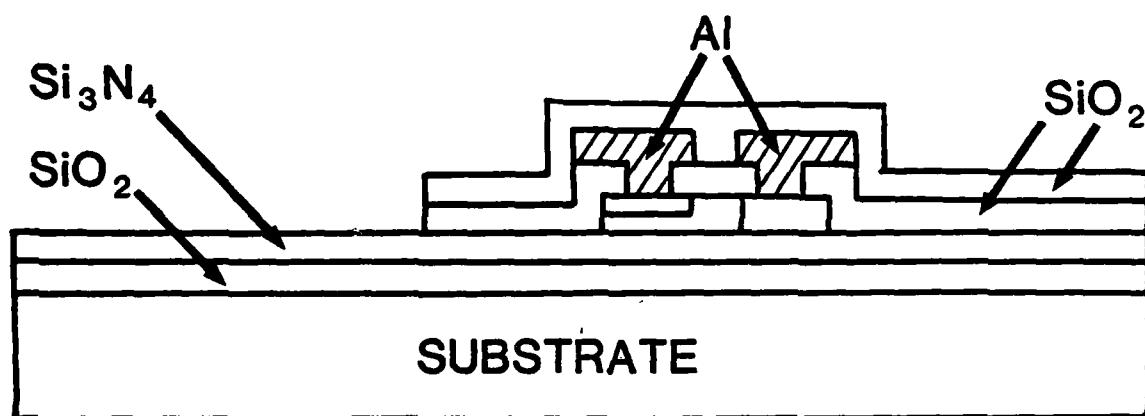


Figure 3. Cross section of one element of the integrated optical photodetector array.

fabricating this test circuitry has been simulated by SUPREM II, and fabrication is beginning. In addition, a model for simulating the band bending of the thin polysilicon layer due to the coupling between the front gate and the underlying substrate has also been underway.

IV. Outlook - Progress with Regard to Objectives

Significant progress towards several of the objectives of the portion of the AFOSR research program for which this interim report applies has been accomplished. An extensive photodetector array test chip has been designed and fabricated on regions of laser recrystallized polysilicon. Success in this area will allow integration of silicon photodetectors onto various optical waveguide substrates. Given the complexity of the design and of the fabrication process, significant progress has been achieved in this area. In the area of SiO_2 waveguides significant progress and accomplishment has taken place with regard to both planar and channel optical waveguides. Although a number of questions remain to be answered, significant progress has been made.

At the present time research in this program is continuing, as described in our most recent proposal.

V. List of Program Publications: AFOSR 81-0130

J.T. Boyd, "Planar and Channel Optical Waveguides Utilizing Silicon Technology," to be presented at and published in The Proceedings of the SPIE Meeting, Cambridge, Massachusetts, October, 1984.

J.T. Boyd, A. Naumaan, R.W. Wu, and D.E. Zelmon, "Integrated Optical Devices Utilizing Silicon," to be presented at and published in The Proceedings of The 1984 National Science Foundation Grantee-User Meeting on Optical Communications, University of California at San Diego, June, 1984.

P.B. Kosel, M.R. Wilson, and J.T. Boyd, "Configurations of High Speed GaAs CCD Imagers," presented at and published in The Proceedings of The Society of Photoinstrumentation Engineers Meeting, Los Angeles, January, 1984.

J.T. Boyd, D.E. Zelmon, H.E. Jackson, and P.B. Kosel, "Properties of Graded-Index SiO₂ Planar Optical Waveguides," presented at the Meeting of the Optical Society of America, New Orleans, October, 1983.

S.H. Chang and J.T. Boyd, "Log-Converting Processor Element for CCD Linear Imaging Arrays," Applied Optics, Vol. 22, pp. 3569-3571, 1983.

S.H. Chang, J.T. Boyd, and J.H. Nevin, "Three Gate MOSFET Providing Independent Control of Transconductance and Output Resistance," IEEE Electron Device Letters, Vol. EDL-4, pp. 289-291, 1983.

C.L. Fan and J.T. Boyd, "Improvement in the Quantum Efficiency of Silicon Photodetectors at Near IR Wavelengths by Edge Illumination," Applied Optics, Vol. 22, pp. 3297-3299, 1983.

S.H. Chang, "Log-Converting CCD Sensor Element and Three Gate MOSFET Device," Ph.D. Dissertation, University of Cincinnati, 1983.

H.E. Jackson, D.E. Zelmon, J.T. Boyd, and P.B. Kosel, "Fabrication of a Graded-Index SiO₂ Planar Optical Waveguide on Silicon Exhibiting Low Scattering," presented at and published in The Proceedings of the Society of Photoinstrumentation Engineers Meeting, Arlington, Virginia, April, 1983.

J.T. Boyd, "Microfabrication Techniques for Integrated Optics," presented at and published in the Proceedings of Electro/83, New York, April, 1983.

D.E. Zelmon, H.E. Jackson, J.T. Boyd, A. Naumaan, and D.B. Anderson, "A Low-Scattering Graded-Index SiO₂ Planar Optical Waveguide Thermally Grown on Silicon," Applied Physics Letters, Vol. 42, pp. 565-566, April 1, 1983.

S. Dutta, H.E. Jackson, J.T. Boyd, and C.W. White, "Rutherford Back Scattering (RBS) Evidence for Solid Phase Laser Annealing of Corning 7059 Glass and ZnO Thin Films," Journal of Applied Physics, Vol. 54, pp. 2125-2126, April, 1983.

S. Dutta, H.E. Jackson, and J.T. Boyd, "Use of Laser Annealing to Achieve Low Loss in Corning 7059 Glass, ZnO, Si₃N₄, Nb₂O₅, and Ta₂O₅ Optical Thin-Film Waveguides," presented at and published in the Proceedings of the Society of Photoinstrumentation Engineers Meeting, Los Angeles, January, 1982.

C.L. Fan, "Improvement in the Performance of Silicon Photodetectors Used in Integrated Optics by Edge Illumination and Optical Waveguide Integration," Ph.D. Dissertation, University of Cincinnati, 1983.

S. Dutta, H.E. Jackson, J.T. Boyd, F.S. Hickernell and R.L. Davis, "Scattering Loss Reduction in ZnO Optical Waveguides by Laser Annealing," Applied Physics Letters, Vol. 39, pp. 206-208, August 1, 1981.

A. Naumaan, D.E. Zelmon, and J.T. Boyd, "A thick SiO₂ Graded-Index Planar Waveguide," presented at and published in the Proceedings of the 31st Electronic Components Conference, Atlanta, May 11-13, 1981.

F.S. Hickernell, R.L. Davis, S. Dutta, J.T. Boyd and H.E. Jackson, "Optical Waveguide Loss Reduction in Zinc Oxide Films by Laser Annealing," presented at and published in the Proceedings of the AIME Electronic Materials Conference, Santa Barbara, June 24-26, 1981.

H. Lu, "CO₂ Laser Recrystallization of Polysilicon and Annealing of MIS Devices," M.S. Thesis, University of Cincinnati, 1982.

S. Dutta, J.T. Boyd, and H.E. Jackson, "Laser Annealing of ZnO Optical Waveguides," presented at the Meeting of the American Physical Society, Dallas, March, 1982.

S. Dutta, H.E. Jackson, and J.T. Boyd, "Use of Laser Annealing to Achieve Low Loss in Corning 7059 Glass, ZnO, Si₃N₄, Nb₂O₅, and Ta₂O₅ Optical Thin-Film Waveguides," presented at and published in the Proceedings of the Society of Photoinstrumentation Engineers Meeting, Los Angeles, January, 1982.

S. Dutta, H.E. Jackson, J.T. Boyd, R.L. Davis, and F.S. Hickernell, "CO₂ Laser Annealing of Si₃N₄, Nb₂O₅, and Ta₂O₅ Thin Film Waveguides to Reduce Optical Scattering," IEEE Journal of Quantum Electronics, Vol. QE-18, pp. 800-806, April, 1982, Joint Special Issue on Optical Guided Wave Technology, also published in IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-30, April, 1982.

J.T. Boyd, S. Dutta, H.E. Jackson, and A. Naumaan, "Reduction of the Effects of scattering by Laser Annealing of Optical Waveguides and by

Use of Integrated Waveguide Detection," Optical Engineering, Vol. 21, pp. 293-295, 1982.

F.K. Hopkins, H.E. Jackson, and J.T. Boyd, "In-Plane Scattering Measurements in a Planar Optical Waveguide by an Integrated Technique," Applied Optics, Vol. 20, pp. 2761-2763, August 15, 1981.

S. Dutta, "Reduction of Scattering in Thin-Film Optical Waveguides by Carbon Dioxide Laser Annealing," Ph.D. Dissertation, University of Cincinnati, 1981.

VI. Acknowledgments

The author would like to acknowledge the contributions of A. Naumaan, D. E. Zelmon, R. W. Wu, H. Lu, and H. A. Timlin to the research described here. The work of H. E. Jackson on most of the projects described has greatly contributed to the degree of success achieved and is appreciated. The author also wishes to acknowledge the skillful work of our microelectronics technicians, J. T. Garrett, and R. Kirschner.

VII. References

1. J.T. Boyd, D.A. Ramey, C.L. Chen, A. Naumaan, S. Dutta and S.H. Chang, "Integration of a Detector Array With An Optical Waveguide Structure and Applications to Signal Processing," Final Report, AFOSR-76-3032, August 7, 1981.
2. D.E. Zelmon, H.E. Jackson, J.T. Boyd, A. Naumaan, and D.B. Anderson, "A Low-Scattering Graded-Index SiO₂ Planar Optical Waveguide Thermally Grown on Silicon," Applied Physics Letters 42, 565 (1983).
3. H.E. Jackson, D.E. Zelmon, J.T. Boyd, and P.B. Kosel, "Fabrication of a Graded-Index SiO₂ Planar Optical Waveguide on Silicon Exhibiting Low Scattering," presented at and published in The Proceedings of the Society of Photoinstrumentation Engineers Meeting, Arlington, Virginia, April, 1983.
4. J.T. Boyd, D.E. Zelmon, H.E. Jackson, and P.B. Kosel, "Properties of Graded-Index SiO₂ Planar Optical Waveguides," presented at the Meeting of the Optical Society of America, New Orleans, October, 1983.
5. M.C. Hamilton, D.A. Wille, and W.J. Miceli, "An Integrated Optical RF Spectrum Analyzer," Optical Engineering 16, 475 (1977).
6. D.B. Anderson, J.T. Boyd, M.C. Hamilton, and R.R. August, "Integrated Optics Approach to the Fourier Transform," IEEE Journal of Quantum Electronics, Vol. QE-13, pp. 268-275, April 1977, Special Issue on Integrated Optics.
7. M.K. Barnoski, B.V. Chen, T.R. Joseph, J.Y.M. Lee, and O.G. Ramer, "Integrated-Optic Spectrum Analyzer," IEEE Trans. on Circuits and Systems CAS-26, 1113 (1979).
8. D. Mergerian, E.C. Malarkey, R.P. Pautienus, J.C. Bradley, G.E. Marx, L.D. Hutcheson, and A.L. Kellner, "Operational Integrated Optical RF Spectrum Analyzer," Appl. Opt. 19, pp. 3033-3034, 1980.
9. T. G. Giallorenzi, J.Z. Bucaro, A. Dandridge, G.H. Sigel, Jr., J.H. Cole, S.C. Rashleigh, and R.G. Priest, "Optical Fiber Sensor Technology," IEEE Journal of Quantum Electronics, Vol. QE-18, p. 626, 1982.
10. D.A. Ramey and J.T. Boyd, "Polyurethane Fan-Out Channel Waveguide Array for High Resolution Optical Waveguide Imaging," IEEE Trans. on Circuits and Systems, Special Issue on Optical Circuits and Systems, Volume CAS-26, pp. 1041-1048, 1979.

11. J.T. Boyd, D.A. Ramey, and C.L. Fan, "Enhanced Optical Waveguide Focal Plane Resolution Utilizing a Channel Waveguide Fan-Out Array Coupled to an Integrated CCD," presented at and published in the Proceedings of the Fifth International Conference on Charge-Coupled Devices, Edinburgh, Scotland, September 12-14, 1979.
12. E.A. Taft, "Index of Refraction of Steam Grown Oxides on Silicon," J. Electrochem. Soc., p. 993, April, 1980 and E.A. Taft, "The Optical Constants of Silicon and Dry Oxygen Oxides of Silicon at 5461A," J. Electrochem. Soc., Solid State Science and Technology 125, p. 968, June, 1978.
13. R.W. Dutton and S.E. Hanson, "Process Modeling of Integrated Circuit Device Technology," Proc. of IEEE 69, p. 1305, 1981.